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Appl. No. 10/605,193  
Amdt. dated February 27, 2006  
Reply to Office action of November 28, 2005

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

- 5 Claim 1 (Currently Amended): A method for locking phase by providing a clock  
synchronized with an input signal, the input signal comprising a plurality of data, the  
method comprising:

generating an estimated rate according to transitions of the input signal;

10 processing a dithering step for updating the estimated rate by multiplying the  
estimated rate by a predetermined ratio;

adjusting a frequency of the clock synchronized with an input signal according to the  
updated estimated rate in the dithering step to make the frequency of the clock  
correspond to the updated estimated rate; and

15 modifying the predetermined ratio so that another dithering step may apply the  
modified predetermined ratio to update the estimated rate[.];

20 wherein before adjusting the frequency of the clock according to the updated  
estimate rate in the dithering step, if a phase difference or frequency difference  
between the clock and the input signal exceeds a predetermined value, the  
frequency of the clock is adjusted according to the updated estimated rate in the  
dithering step.

Claim 2 (Original): The method of claim 1 wherein the predetermined ratio will not vary  
with the change of the estimated rate in the dithering step when processing the  
dithering step.

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Claim 3 (Original): The method of claim 1 further comprising changing the predetermined ratios of the adjacent dithering steps according to a predetermined rule.

Claim 4 (Original): The method of claim 1 further comprising:

5 obtaining a sampling clock wherein the sampling clock comprises a plurality of sampling cycles;

generating the input signal according to a signal level of a data signal corresponding to the sampling cycles in the sampling clock; and

10 generating the estimated rate according to the number of the sampling cycles in a predetermined period of time and the number of the changes of the signal level of the input signal in the predetermined period of time.

Claim 5 (Currently Amended): The method of claim 1 wherein before adjusting the frequency of the clock according to the updated estimate rate in the dithering step, a judgment step is processed according to [[a]] the phase difference or frequency  
15 difference between the clock and the input signal to decide whether the frequency of the clock is adjusted according to the updated estimated rate in the dithering step.

Claim 6 (Cancelled):

Claim 7 (Original): The method of claim 5 wherein in the judgment step, if the phase difference or the frequency difference between the clock and the input signal is  
20 lower than a predetermined value, the frequency of the clock is not adjusted according to the updated estimated rate in the dithering step.

Claim 8 (Currently Amended): A phase lock circuit for providing a clock synchronized with an input signal, the input signal comprising a plurality of data, the phase lock

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circuit comprising:

a measuring module for generating an estimated rate according to transitions of the input signal;

5 a dithering module coupled to the measuring module for updating the estimated rate by multiplying the estimated rate by a predetermined ratio; [[and]]

an oscillator for adjusting a frequency of the clock synchronized with an input signal according to the updated estimated rate in the dithering module to make the frequency of the clock correspond to the updated estimated rate; and

10 an error-test module for generating a frequency adjustment value according to phase difference or frequency difference between the clock and the input signal wherein when the phase difference or the frequency difference between the clock and the input signal is lower than a predetermined value, the updated estimated rate of the dithering module ceases to be transmitted to the oscillator and the frequency adjustment value of the error-test module is transmitted to the  
15 oscillator, so that the oscillator can adjust the frequency of the clock according to the frequency adjustment value;

20 wherein after the dithering module updates the estimated rate, the predetermined ratio is modified to multiply the estimated rate by a modified predetermined ratio for updating the estimated rate in the dithering module when the dithering module generates another updated estimated rate.

Claim 9 (Original): The phase lock circuit of claim 8 wherein the predetermined ratio of the dithering module will not vary with the change of the estimated rate of the measuring module.

Claim 10 (Original): The phase lock circuit of claim 8 wherein the dithering module

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modifies the predetermined ratio after the estimated rate is updated according to a predetermined rule, so that the modified predetermined ratio can be used when the estimated rate is updated the next time.

Claim 11 (Original): The phase lock circuit of claim 8 further comprising:

5 a converter for receiving a sampling clock that comprises a plurality of sampling cycles and for generating the input signal according to a signal level of a data signal corresponding to the sampling cycles in the sampling clock;

wherein the measuring module generates the estimated rate according to the number of the sampling cycles in a predetermined period of time and the number of the  
10 changes of the signal level of the input signal.

Claim 12 (Original): The phase lock circuit of claim 8 further comprising a detecting circuit for deciding whether the updated estimated rate of the dithering module is transmitted to the oscillator to adjust the frequency of the clock according to a phase difference or frequency difference between the clock and the input signal.

15 Claim 13 (Original): The phase lock circuit of claim 12 wherein if the detecting circuit detects that the phase difference or the frequency difference between the clock and the input signal exceeds a predetermined value, the updated estimated rate of the dithering module is transmitted to the oscillator.

Claim 14 (Cancelled)

20 Claim 15 (Currently Amended): A method for locking phase by providing a comparing clock synchronized with an input signal, the input signal comprising a plurality of data, the method comprising:

generating a frequency adjustment value according to the input signal;

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generating a dithering estimated value according to the input signal through a  
dithering step;

5        setting a dithering estimated value as a new comparing clock when a synchronization  
error between the comparing clock and the input signal exceeds a  
predetermined value; [[and]]

setting the frequency adjustment value as the new comparing clock when the  
synchronization error between the comparing clock and the input signal does  
not exceed the predetermined value; and

10        comparing the new comparing clock with the input signal in order to adjust the new  
comparing clock.

Claim 16 (Original): The method of claim 15 wherein the dithering step is used to  
generate an estimated rate according to transitions of the input signal and to generate  
the dithering estimated value by multiplying the estimated rate by a predetermined  
ratio.

15        Claim 17 (Original): The method of claim 16 wherein the predetermined ratio will not  
vary with the change of the estimated rate in the dithering step.

Claim 18 (Original): The method of claim 16 wherein the predetermined ratio of the  
adjacent dithering step is changed according to a predetermined rule.

20        Claim 19 (Original): The method of claim 15 further comprising adjusting the frequency  
of the comparing clock according to a phase difference or frequency difference  
between the comparing clock and the input signal.

Claim 20 (Original): The method of claim 15 further comprising: generating an estimated  
rate according to the number of sampling cycles in a predetermined period of time

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and the number of the changes of signal level of the input signal in the  
predetermined period; and generating the dithering estimated value in the dithering  
step according to the estimated rate.